SEMICONDUCTOR MEMORY DEVICE HAVING ECC TYPE ERROR RECOVERY CIRCUIT

Abstract of the Disclosure

A semiconductor memory device having an error check and correction (ECC) type error recovery circuit in which disposition of ECC cells is improved. The memory device comprises: a memory cell array including a plurality of normal cell array portions and an ECC cell array portion; an X decoder for selecting one of word lines in the memory cell array, the word lines extending from the X decoder to the memory cell array; an ECC operation circuit for performing error check and correction based on cell data read out from a selected word line, the cell data including data from normal cells and ECC cells of the selected word line. The ECC memory cell array portion is disposed at a location other than the far end of the word lines from the X decoder, that is, the ECC cell array portion is disposed at a location in which read out speed of data from ECC cell or cells does not become the worst speed in the memory device. Therefore, the worst data read out speed can be measured from outside.